



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,438	11/12/2003	Torsten Partsch	2003PS2601US/I331.102.101	7153
7590	09/20/2006			EXAMINER
Dicke, Billig & Czaja, PLLC Fifth Street Towers Suite 2250 100 South Fifth Street Minneapolis, MN 55402			MCFADDEN, MICHAEL B	
			ART UNIT	PAPER NUMBER
			2188	
			DATE MAILED: 09/20/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/706,438	PARTSCH, TORSTEN
	Examiner Michael B. McFadden	Art Unit 2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 05 July 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-38 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-38 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 12 November 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Status of Claims

1. Claims 1-38 are pending in the Application.

Response to Amendment

2. Applicant's arguments filed on 05 July 2006 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 17, 18, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Usami (US Patent No. 6,205,516).

5. **Regarding Claims 1 - 3, 17, 18, and 31,** Usami discloses a random access memory, comprising: an array of memory cells; a memory configured to receive data from the array of memory cells; a bypass circuit configured to receive the data from the array of memory cells and to bypass the memory; and a circuit configured to select

between receiving the data from the memory to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency signal. Also, the random access memory, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency signal indicates a column address strobe latency value of one. Lastly, when the random access memory, wherein the circuit is configured to receive the data from the bypass circuit and provide the second output signals if the column address strobe latency select signal indicates a column address strobe latency value of one. (See Figure 2 and Figure 4)

Usami discloses a programmable SDRAM. An SDRAM is inherently created from a memory array, a memory configured to receive data from the array, a bypass circuit, and a circuit that will select the programmed mode. Figure 4 shows that depending on the contents of the CAS Latency bits A4, A5, and A6 the CL (CAS Latency) will vary accordingly as described in Claims 2 and 3.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Art Unit: 2188

7. Claims 4-16, 19-30 and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usami (US Patent No. 6,205,516).

8. **Regarding Claims 4-11, 19-21, 25-30, and 33-38,** Usami discloses circuits configured to receive first rise and fall signals to serialize the data following a read command initiated by an edge of a clock cycle. (**See Figures 2 and 4.**)

9. **A programmable SDRAM must inherently contain circuit means for serializing data as initiated by an edge of a clock cycle. The Examiner takes official notice that any combination of clock edges can be combined to provide the instruction to receive data. The motivation for doing so would be to increase system speed for read and write commands. Therefore it would be obvious to use any combination of clock edges to provide the instruction to receive data so that the system can be configured to increase system speed for read and write commands to obtain the invention claimed.**

10. **Regarding Claims 12-16, 22-24, and 32,** Usami fails to disclose a tri-state output, a first in/first out memory, a low power synchronous dynamic random access memory, a double data rate-I synchronous dynamic random access memory, a double data rate-II synchronous dynamic access memory, a data delay circuit, and an off chip driver.

However, it would have been obvious for a person of ordinary skill in the art to combine these limitations with the random access memory of Usami.

The motivation for doing so would have been that using tri-states, FIFO memory, low power SDRAM, DDR1 SDRAM, DDR2 SDRAM, delay circuits, and off chip drivers

in random access memory devices is an efficient way to utilize system resources along with expediting memory requests.

Therefore it would have been obvious for a person of ordinary skill in the art to combine the use of tri-states, FIFO memory, low power SDRAM, DDR1 SDRAM, DDR2 SDRAM, delay circuits, or off chip drivers with the random access memory of Usami, for the benefit of efficiently utilizing system resources along with expediting memory requests to obtain the invention claimed.

Response to Arguments

11. Applicant's arguments filed 05 July 2006 have been fully considered but they are not persuasive.

12. **Regarding Claims 1 - 3, 17, 18, and 31,** Applicant contends that Usami does not disclose a bypass circuit or a circuit configured to select between receiving the data from the memory array to provide first output signals and receiving the data from the bypass circuit to provide second output signals based on a column address strobe latency select signal as recited in claim 1. However, as previously stated Usami teaches varying CAS Latencies (CLs). Cache Latencies are varied by changing the number of pipeline stages in the cache. A CL of one means that a cache has one pipeline stage, a CL of two means two pipeline stages, and so on. Therefore, in providing multiple CLs Usami inherently teaches bypassing one or more pipeline stages based on setting of the CAS Latency bits. In bypassing a pipeline

stage, a bypass circuit and a circuit configured to select between receiving data are inherent.

13. **Regarding Claims 4-11, 19-21, 25-30, and 33-38,** Applicant contends that any combination of clock edges being combined to provide the instruction to receive data is not a well known fact and has requested a reference to teach the limitation. **However, using Fetterman et al. ((US Patent No. 5,553,256) herein after Fetterman) and Sharma et al. ((US Patent No. 5,829,016) herein after Sharma), as evidentiary support, the limitations are taught.** Fetterman (Column 15, Lines 9-14) teaches a read command which coincides with the rising edge of a clock cycle. While Sharma (Column 10, Lines 19-21) teaches a read command which begins on the falling edge. Therefore either rising or falling clock edges can be used to provide an instruction to receive data.

14. **Regarding Claims 12-16, 22-24, and 32,** Applicant contends that a tri-state output, a first in/first out memory, a low power synchronous dynamic random access memory, a double data rate-I synchronous dynamic random access memory, a double data rate-II synchronous dynamic access memory, a data delay circuit, and an off chip driver are not well known facts and has requested a reference to teach the limitations. **However, a tri-state output is taught using Cochran (US Patent No. 3,958,223) as evidentiary support. (Cochran: Column 11, Lines 64-68.) A first in/first out memory is taught by Altman (US Patent No. 3,593,286). (Altman: Column 9, Lines**

73-75). A low power synchronous random access memory, otherwise known as low power SDRAM, is taught by Bunker (US Patent No. 6,469,474.) (Bunker: Column 8, Lines 54-56) A double data rate-I synchronous dynamic random access memory, otherwise known as DDR-I SDRAM, is taught by Tien et al ((US Patent No. 5,923,613) herein after Tien.) (Tien: Column 3, Lines 55-58.) A double data rate-II synchronous dynamic random access memory, otherwise known as a DDR-II SDRAM, is taught by Hovis et al. ((US Patent No. 6,434,082) herein after Hovis.) (Hovis: Column 7, Line 60 – Column 8, Line 16.) A data delay circuit is taught by Benowitz et al. ((US Patent No. 3,614,317) herein after Benowitz) (Benowitz: Column 4, Lines 60-63.) An off chip driver is taught by Cox et al. ((US Patent No. 3,987,287) herein after Cox) (Cox: Column 7, Lines 12-25.) The respective limitations have been taught using the sited patents as evidentiary references.

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Reginald J. Bragdon

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

MBM
09/06/2006